**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Applicant : Hsueh-Yuan Pao et al.   Docket No. : IL-11028

Serial No. : 10/644,561   Art Unit: 2611

Filed : August 19, 2003   Examiner: E. File

For : Digital Intermediate Frequency QAM
Modulator Using Parallel Processing

BRIEF ON APPEAL

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This is an appeal to the Board of Patent Appeals and Interferences from the final rejection of claims 1-12 mailed January 16, 2007. On July 16, 2007, a timely Notice of Appeal was filed.

I. REAL PARTIES IN INTEREST

The real parties in interest are the Regents of the University of California and the United States of America as represented by the United States Department of Energy.

II. RELATED APPEALS AND INTERFERENCES

Appellant knows of no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-12 are pending on appeal and stand rejected. The rejection of claims 1-12 is appealed. A copy of the claims on appeal is set forth in the Claims Appendix.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent apparatus claims 1, 2, 4 and 6 claim a digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier. Independent method claims 7, 8, 10 and 12 claim a method for processing data with a digital intermediate frequency QAM modulator using parallel processing without the use of a multiplier.

As shown in Figure 3 and described in paragraphs 35 and 36 in the published patent application, independent claim 1 provides a serial-to-parallel data converter **300** to convert a string of serial data to a plurality of parallel data; an I and Q mapper **400** to determine the I and Q locations of the data; a plurality of look-up-tables (LUTs) **800** to **803** and **820** to **823** operatively connected to receive and store the I and Q locations; a plurality of adders **113** to **116** to add the storred I and Q locations; a plurality of registers **124** to **127** to collect and store the output data; and a digital to analog converter **200** to convert the output data to analog data. Claim 7 embodies the method of operation of the apparatus of claim 1, and it is also described in paragraphs 35 and 36 with reference to Figure 3.

Independent claim 2 includes the elements of claim 1 and additionally includes multiplexers to collect odd and even subscript output data from the registers, as shown in figures 3, 5 and 6A-6E and described in paragraphs 35, 36 and 51. Claim 7 embodies the method of operation of the apparatus of claim 2,

and it is also described in paragraphs 35, 36 and 51 with reference to figures 3, 5 and 6A-6E.

Independent claim 4 includes all of the elements of independent claim 2 without specifically reciting the serial-to-parallel data converter or the I and Q mapper. Claim 10 embodies the method of operation of the apparatus of claim 4 See paragraph 35, 36 and 51 and figures 3, 5 and 6A-6E.

Independent claim 6 includes all of the elements of independent claim 1 without specifically reciting the serial-to-parallel data converter or the I and Q mapper. Claim 12 embodies the method of operation of the apparatus of claim 6 See paragraph 35, 36 and 51 and figures 3, 5 and 6A-6E.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-12 are unpatentable over Zhang in view of McCullough.

VII. ARGUMENT

Are claims 1-12 unpatentable over Zhang in view of McCullough?

The Examiner admits that Zhang fails to disclose a quadrature amplitude modulator that does not include a multiplier. All of the independent claims in the present application under appeal specifically exclude the use of a multiplier. The Examiner relies upon the secondary reference to exclude the use of the multiplier. McCullough teaches a biphase modulator and fails to teach amplitude modulation. McCullough's teachings are only valid for phase-shift keying (PSK)

applications, not Quadrature Amplitude Modulation (QAM), which is the subject of Zhang and is claimed in all of the independent claims of the present invention (claims 1, 2, 4, 6-8, 10 and 12). McCullough does not teach a modulator that can function in the QAM mode. One skilled in the art would not incorporate McCullough's modulation technique into Zhang's invention. Therefore the rejection of claims 1, 2, 4, 6-8, 10 and 12 should be withdrawn. The rejection of claims 3, 5, 9 and 11 should be withdrawn because they depend from claims 2, 4, 8 and 10, respectively. Therefore the rejection should be withdrawn.

In the non-final rejection mailed May 17, 2006, the Examiner states: "<u>McCullough teaches a modulator which can function in a variety of modes including quadrature amplitude modulation and does not disclose the use of any modulators.</u>" (The applicants understand that the Examiner's second use of the term "modulators" in the foregoing sentence was intended to be "multipliers.") Thus, the Examiner argues that one skilled in the art would combine the two references based on two premises. His first premise is that McCullough can function in the quadrature amplitude modulation mode. His second premise is that McCullough does not disclose the use of any multipliers. The applicants responded with a declaration that refuted the Examiner's first premise. McCullough does not teach a modulator that can function in a QAM mode. The only mention of QAM by McCullough is in the Background section, where it mentions that QAM suffers from a lack of flexibility in choosing modulation angles. In the Final Office Action, the Examiner takes the new position that his

first premise was not necessary to make the combination, and that he never

relied on that premise in the above referenced non-final office action. The

applicants respectfully disagree. His own words, as shown above, clearly base

his justification for the combination of the two references on the two discussed

premises. The applicants refuted one of his premises in the attached Declaration,

filed with the response to the non-final office action. Therefore, the examiner

should have at least provided a new non-final office action or should have

allowed the claims.

Accordingly it is submitted that the rejections of claims 1-12 are improper and

should be reversed.

Respectfully submitted,

/John P. Wooldridge #38,725/
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Registration No. 38,725
Dated: September 17, 2007   Tel. No. 808-875-0012

VIII. CLAIMS APPENDIX

1. A digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier, comprising:

a serial-to-parallel data converter operatively connected to receive serial data, wherein said serial-to-parallel data converter converts a string of serial data to a plurality of parallel data;

an I and Q mapper operatively connected to receive said plurality of parallel data and determine its I and Q locations;

a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said

output data comprising IQ_1 to IQ_{IQN} to analog data, wherein said Quadrature

Amplitude Modulation modulator does not include a multiplier.

2. A digital intermediate frequency Quadrature Amplitude

Modulation modulator using parallel processing without the use of a multiplier,

comprising:

a serial-to-parallel data converter operatively connected to receive

serial data, wherein said serial-to-parallel data converter converts a string of

serial data to a plurality of parallel data;

an I and Q mapper operatively connected to receive said plurality of

parallel data and determine its I and Q locations;

a plurality of look-up-tables (LUTs) operatively connected to receive

and store said I and Q locations, wherein the I LUTs are configured I_1 to I_n,

wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the

Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of

said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I

and Q locations stored within said plurality of LUTs, wherein said plurality of

adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of

said plurality of adders, wherein each I and Q having a particular subscript are

added in the adder having the same subscript to produce output data comprising

IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said

output data comprising IQ_1 to IQ_{IQN};

at least one multiplexer operatively connected to collect from said

plurality of registers the subscript output data comprising only odd subscript

output data from said output data comprising IQ_1 to IQ_{IQN};

at least one multiplexer operatively connected to collect from said

plurality of registers the subscript output data comprising only even subscript

output data from said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said odd

subscript data and said even subscript data to analog data, wherein said

Quadrature Amplitude Modulation modulator does not include a multiplier.

3. The digital intermediate frequency Quadrature Amplitude

Modulation modulator using parallel processing without the use of a multiplier

of claim 2, wherein said at least one multiplexer operatively connected to collect

from said plurality of registers the subscript output data comprising only odd

subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises

nx2 multiplexers, where n is an integer, and wherein said at least one multiplexer

is operatively connected to collect from said plurality of registers the subscript

output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers.

4. A digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier, comprising:

a plurality of look-up-tables (LUTs) operatively connected to receive and store I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN};

a first multiplexer operatively connected to collect from said plurality of registers only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

a second multiplexer operatively connected to collect from said

plurality of registers only even subscript output data from said output data

comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said odd

subscript data and said even subscript data to analog data, wherein said

Quadrature Amplitude Modulation modulator does not include a multiplier.

5. The digital intermediate frequency Quadrature Amplitude

Modulation modulator using parallel processing without the use of a multiplier

of claim 4, wherein said first multiplexer comprises nx2 multiplexers, where n is

an integer, and wherein said second multiplexer comprises nx2 multiplexers.

6. A digital intermediate frequency Quadrature Amplitude

Modulation modulator using parallel processing without the use of a multiplier,

comprising:

a plurality of look-up-tables (LUTs) operatively connected to receive

and store I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N

is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs

are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said

plurality of LUTs;

a plurality of adders operatively connected to receive and add said I

and Q locations stored within said plurality of LUTs, wherein said plurality of

adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said output data comprising IQ_1 to IQ_{IQN} to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

7. A method for processing data with a digital intermediate frequency QAM modulator using parallel processing without the use of a multiplier, comprising:

receiving and converting a string of serial data into a plurality of parallel data;

determining the I and Q locations of said plurality of parallel data;

storing said I and Q locations in a plurality of look-up-tables (LUTs), wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding said I and Q locations stored within said plurality of LUTs, wherein ~~said~~ a plurality of adders are configured A_1 to A_{AN},

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wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing said output data comprising IQ_1 to IQ_{IQN} in a plurality of registers; and

converting said output data comprising IQ_1 to IQ_{IQN} to analog data in a digital to analog converter, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

8. A method for processing data in a digital intermediate frequency QAM modulator using parallel processing without the use of a multiplier, comprising:

receiving and converting a string of serial data to a plurality of parallel data;

receiving said plurality of parallel data in an I and Q mapper and determine the I and Q locations of said plurality of parallel data;

receiving and storing said I and Q locations in a plurality of look-up-tables (LUTs), wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding said I and Q locations stored within said plurality of LUTs in a plurality of adders, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN};

collecting, in a first multiplexer, from said plurality of registers, the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

collecting, in a second multiplexer, from said plurality of registers, the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

converting, a digital to analog converter, said odd subscript data and said even subscript data to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

9. The method of claim 8, wherein said first multiplexer comprises nx2 multiplexers, where n is an integer, and wherein said second multiplexer omprises nx2 multiplexers.

10. A method for processing data in a digital intermediate frequency QAM modulator using parallel processing without the use of a multiplier, comprising:

receiving and storing in a plurality of look-up-tables (LUTs), I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding in a plurality of adders said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN};

collecting in a first multiplexer only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

collecting in a second multiplexer only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

converting in a digital to analog converter said odd subscript data and said even subscript data to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

11. The method of claim 10, wherein said first multiplexer comprises nx2 multiplexers, where n is an integer, and wherein said second multiplexer comprises nx2 multiplexers.

12. A method for processing data with a digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier, comprising:

receiving and storing, in a plurality of look-up-tables (LUTs) I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding in a plurality of adders said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN}; and

converting in a digital to analog converter said output data comprising

IQ_1 to IQ_{IQN} to analog data, wherein said Quadrature Amplitude Modulation

modulator does not include a multiplier.

IX. <u>EVIDENCE APPENDIX</u>

The following Declaration was entered into the record on October 20, 2006.
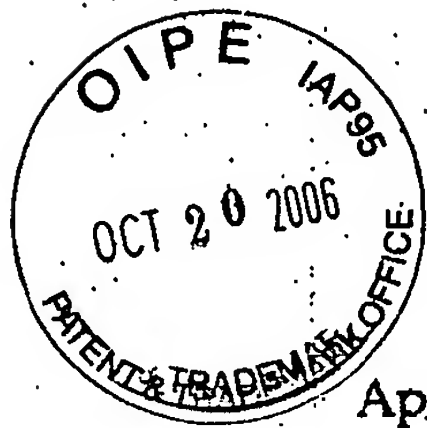
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hsueh-Yuan Pao et al. Attorney Docket No. : IL-11028

Serial No. : 10/644,561 Art Unit: 2611

Filed : August 19, 2003 Examiner: E. File

For : Digital Intermediate Frequency QAM
Modulator Using Parallel Processing

DECLARATION UNDER 37 CFR §1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Hsueh-Yuan Pao, hereby declare that I am a citizen of the United States

of America and a resident of Livermore, California.

I have a PhD in _1995____ from the University of Arizona____.

I have worked in the field of _electrical engineering_____ at Lawrence

Livermore National Laboratory for __8___ years.

I have read the office action and would like the examiner to consider my

comments concerning the inapplicability of the teachings of the McCullough

reference to the Zhang reference.

McCullough's invention is a biphase modulator as indicated in the title.

There is no teaching of amplitude modulation in this reference. McCullough's

teachings are only valid for phase-shift keying (PSK) applications, not Quadrature

Amplitude Modulation (QAM), which is the subject of Zhang and is claimed in the

present invention. McCullough's invention only varies phase, not amplitude. QAM

requires modulation of amplitude. In QAM, the amplitude of two waves, 90 degress

out-of-phase with each other are modulated to represent the data signal. In phase-

shift keying, the amplitude of the modulating signal is constant, and only the phase

is varied. Contrary to the Examiner's assertion, McCullough does not teach a

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modulator that can function in the QAM mode. Thus, one skilled in the art would not incorporate McCullough's modulation technique into Zhang's invention.

Accordingly, I respectfully request that the rejections be withdrawn.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Dated: September 15, 2006

Hsueh-Yuan Pao

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X. RELATED PROCEEDINGS APPENDIX

None